What is claimed is:

1.   A branch predicting device, comprising:

a storing circuit storing information specifying
5   a return address of a subroutine when an instruction
equivalent to a subroutine call is detected;

a comparing circuit making a comparison between
information specifying a branch destination address
of   an   instruction   which   can   possibly   be   an
10   instruction equivalent to a subroutine return and the
information specifying the return address stored in
said storing circuit, and outputting a result of the
comparison, when the instruction which can possibly
be   the   instruction   equivalent   to   the   subroutine
15   return is detected; and

an   identifying   circuit   identifying   an
instruction equivalent to a subroutine return, which
corresponds   to   the   instruction   equivalent   to   the
subroutine   call,   based   on   the   result   of   the
20   comparison.

2.   The branch predicting device according to
claim 1, wherein

said storing circuit stores a register number of
25   a   link   register,   which   is   specified   by   the

instruction equivalent to the subroutine call, as the information specifying the return address.

3. The branch predicting device according to claim 1, wherein

said storing circuit stores the return address of the subroutine as the information specifying the return address.

4. A branch predicting device, comprising:

a stack circuit storing information specifying a return address of a subroutine;

a push circuit pushing the information specifying the return address onto said stack circuit, when an instruction equivalent to a subroutine call is detected;

a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the

5   comparison.

5.   The branch predicting device according to claim 4, wherein:

said push circuit pushes a register number of a

10   link register, which is specified by the instruction equivalent to the subroutine call, onto said stack circuit as the information specifying the return address;

said comparing circuit makes a comparison

15   between a register number of a branch destination address register, which is specified by the instruction which can possibly be the instruction equivalent to the subroutine return, and a register number stored in the top entry of said stack circuit;

20   and

said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return when

25   the compared register numbers match.

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6.   The branch predicting device according to claim 5, wherein

said identifying circuit identifies the instruction which can possibly be the instruction

5   equivalent to the subroutine return as the instruction equivalent to the subroutine return regardless of the result of the comparison, if the register number of the branch destination address register corresponds to a particular register.

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7.   The branch predicting device according to claim 5, wherein

said push circuit does not push the register number of the link register onto said stack circuit

15   if the register number of the link register corresponds to a particular register.

8.   The branch predicting device according to claim 4, further comprising

20   a pop circuit popping said stack circuit when said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return, and a branch by the

25   instruction equivalent to the subroutine return is

taken.

9. The branch predicting device according to claim 1, further comprising

5   a predicting circuit storing branch history information for a branch prediction, wherein

said comparing circuit makes the comparison between the information specifying the branch destination address and the information specifying

10   the return address, when the branch history information is registered to said predicting circuit.

10. The branch predicting device according to claim 1, further comprising

15   a circuit invalidating the information stored in said storing circuit when an event which causes a correspondence between a subroutine call and a subroutine return to be improper.

20   11. The branch predicting device according to claim 1, further comprising:

a predicting circuit storing branch history information for a branch prediction; and

a setting circuit setting in said predicting

25   circuit a flag indicating that a return destination

of a detected instruction equivalent to a subroutine return differs, when an instruction equivalent to a subroutine return, which does not return to an instruction address immediately succeeding the instruction equivalent to the subroutine call, is detected.

12. The branch predicting device according to claim 11, wherein

said predicting circuit comprises a return address stack circuit storing the return address of the subroutine, pops said return address stack circuit if the flag is recognized at the time of a branch prediction, and does not use a popped return address as a predicted branch destination.

13. The branch predicting device according to claim 1, further comprising:

a predicting circuit storing branch history information for a branch prediction; and

a circuit performing a control such that a predetermined flag is set when an instruction equivalent to a subroutine call, which is unregistered to said predicting circuit, is detected, the predetermined flag is reset when an instruction

equivalent to a subroutine return, which corresponds to the unregistered instruction equivalent to the subroutine call, is detected, and the instruction equivalent to the subroutine return corresponding to

5   the unregistered instruction is not identified as an instruction equivalent to a subroutine return in said predicting circuit.

14.   A branch predicting device, comprising:

10   a return address stack circuit storing a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

         a comparing circuit making a comparison between a branch destination address of an instruction which

15   can possibly be an instruction equivalent to a subroutine return, and the return address stored in said return address stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the

20   subroutine return is detected; and

         an   identifying   circuit   identifying   an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the

25   comparison.

15. A branch predicting method, comprising:

registering information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

5   making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the registered information specifying the return address, when the

10   instruction which can possibly be the instruction equivalent to the subroutine return is detected;

identifying the instruction which can possibly be the instruction equivalent to the subroutine return as an instruction equivalent to a subroutine

15   return, which corresponds to the instruction equivalent to the subroutine call, if the information specifying the branch destination address and the information specifying the return address match;

identifying the instruction which can possibly

20   be the instruction equivalent to the subroutine return not as the instruction equivalent to the subroutine return, which corresponds to the instruction equivalent to the subroutine call, if the information specifying the branch destination address

25   and the information specifying the return address do

not match; and

making a branch prediction by using an identification result.

5 16. A branch predicting device, comprising:

storing means for storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

comparing means for making a comparison between
10 information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing means, and for outputting a result of
15 the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

identifying means for identifying an instruction equivalent to a subroutine return, which corresponds
20 to the instruction equivalent to the subroutine call, based on the result of the comparison.

17. A branch predicting device, comprising:

stack means for storing information specifying
25 a return address of a subroutine;

push means for pushing the information specifying the return address onto said stack means, when an instruction equivalent to a subroutine call is detected;

5   comparing means for making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in

10   a top entry of said stack means, and for outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected; and

identifying means for identifying an instruction

15   equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison.

18. A branch predicting device, comprising:

20   return address stack means for storing a return address of a subroutine when an instruction equivalent to a subroutine call is detected;

comparing means for making a comparison between a branch destination address of an instruction which

25   can possibly be an instruction equivalent to a

subroutine return, and the return address stored in said return address stack means, and for outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to

5   the subroutine return is detected; and

identifying means for identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison.